WHAT IS CLAIMED IS

1. A correlation and demodulation circuit for a receiver for signals modulated by a first code of a determined repetition length, said first code defining a source transmitting said signals, said circuit including a correlation stage connected to control means in particular for configuring said correlation stage in normal operating mode or in test mode, in normal operation said stage being intended to receive intermediate signals corresponding to the modulated signals shaped in receiver modulated signal receiving means, said intermediate signals being correlated in a correlator control loop of said correlation stage with a replica of the first code supplied by a code generator, wherein in test phase, said code generator is adapted via control means to generate a replica of a second repetition code shorter than the first code for correlation operations with intermediate test signals modulated by the second code of shorter repetition length than the first code and supplied to the correlation stage so as to perform a test representative of the correlation stage in closed loop operation more quickly than with signals modulated by the first code.

2. A correlation and demodulation circuit according to claim 1, wherein it includes a test signal generator capable of supplying, in test phase, the intermediate test signals to the correlation stage instead of intermediate signals from the receiver, said test signals being modulated by the second code of shorter repetition length than the first code so as to perform a test representative of the correlation stage in closed loop operation.

3. A correlation and demodulation circuit according to claim 2, for a radio-frequency signal receiver, the first code being a first pseudo-random code which is different for each transmitting satellite, wherein the test signal generator supplies, in test phase, test signals modulated by a second pseudo-random code of shorter repetition length than the first pseudo-random code, and wherein the code generator is adapted via control means to generate a replica of the second pseudo-random code for the correlating operations with the test signals in test phase.

4. A correlation and demodulation circuit according to claim 3 for a GPS type receiver, wherein the control means form part of microprocessor means capable of calculating position, speed and time data, adapting control loop parameters at the beginning of the correlation operations and checking that the correlation stage works properly in test phase.

5. A correlation and demodulation circuit according to claim 3, wherein the correlation stage includes several channels each of which is provided with a correlator to allow several visible satellites to be acquired and tracked simultaneously in normal

operation, whereas in test phase all the correlation stage channels, in which each code generator is adapted to generate the same second code replica, receive only the test signals from the test signal generator in order to check simultaneously that the correlating operations of all the correlation stage channels are working properly.

6. A correlation and demodulation circuit according to claim 4, wherein the microprocessor is programmed so as to command the test phase of the correlation stage at predetermined periods of time.

7. A correlation and demodulation circuit according to claim 3, wherein the test signal generator generates, in test phase, carrier frequency test signals modulated by the second pseudo-random code whose repetition length is determined so as to take into account, in control loops relating to the carrier frequency and to the pseudo-random code of the correlation stage, of inherent noise in the radio-frequency signals modulated by the first pseudo-random code, in order to have a comparable power with the output signals from pre-detection elements, such as integrator counters.

8. A correlation and demodulation circuit according to claim 7, wherein the microprocessor means define, in collaboration with the code generator of each channel of the correlation stage, the pre-detection element integration duration as a function of the repetition length of the first or second pseudo-random code.

9. A correlation and demodulation circuit according to claim 3, wherein the test signal generator includes a second pseudo-random code generator, a first numerically controlled oscillator, such as an 8-bit oscillator, for supplying clock signals to the second pseudo-random code generator on the basis of a first binary word provided by the microprocessor means, a second numerically controlled oscillator, such as an 8-bit oscillator, for generating carrier frequency signals on the basis of a second binary word provided by the microprocessor means, the second pseudo-random code being modulated on said carrier frequency signals, and a message generator whose message signals are also modulated on the carrier frequency signals, the correlation stage being intended to supply test message data to the microprocessor means for the closed loop operating test phase check of the correlation stage.

10. A correlation and demodulation circuit according to claim 7, wherein the reduced second pseudo-random code has a repetition length equal to 31, whereas the first pseudo-random code of the radio-frequency signals has a repetition length equal to 1023 allowing the supply, at one output of the correlation stage pre-detection elements, comparable signals taking account of inherent noise in the radio-frequency signals.

11. A correlation and demodulation circuit according to claim 3, wherein the correlation stage includes, for each channel, a controller connected to the correlator for implementing an algorithm for processing the digital signals in all the synchronisation tasks in order to adjust in particular phase and/or frequency parameters for the code generator in a normal operating mode or in a test mode.

12. A correlation and demodulation circuit according to claim 5, wherein the correlator of each channel of the correlation stage includes means for generating a replica of carrier frequency signals able to be adapted by the microprocessor means in a normal operating mode or in a test mode, as a function of the carrier frequency of the intermediate signals supplied to the correlator.

13. A correlation and demodulation circuit according to claim 1, wherein all the elements of said circuit are made on a single semiconductor substrate, such as a silicon substrate.